

NTJD1155L

Power MOSFET

8 V, ±1.3 A, High Side Load Switch with Level-Shift, P-Channel SC-88

The NTJD1155L integrates a P and N-Channel MOSFET in a single package. This device is particularly suited for portable electronic equipment where low control signals, low battery voltages and high load currents are needed. The P-Channel device is specifically designed as a load switch using ON Semiconductor state-of-the-art trench technology. The N-Channel, with an external resistor (R1), functions as a level-shift to drive the P-Channel. The N-Channel MOSFET has internal ESD protection and can be driven by logic signals as low as 1.5 V. The NTJD1155L operates on supply lines from 1.8 to 8.0 V and can drive loads up to 1.3 A with 8.0 V applied to both V_{IN} and $V_{ON/OFF}$.

Features

- Extremely Low $R_{DS(on)}$ P-Channel Load Switch MOSFET
- Level Shift MOSFET is ESD Protected
- Low Profile, Small Footprint Package
- V_{IN} Range 1.8 to 8.0 V
- ON/OFF Range 1.5 to 8.0 V
- ESD Rating of 3000 V
- Pb-Free Package is Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit
Input Voltage (V_{DSS} , P-Ch)		V_{IN}	8.0	V
ON/OFF Voltage (V_{GS} , N-Ch)		$V_{ON/OFF}$	8.0	V
Continuous Load Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_L	±1.3
		$T_A = 85^\circ\text{C}$		±0.9
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	0.40
		$T_A = 85^\circ\text{C}$		0.20
Pulsed Load Current	$t_p = 10 \mu\text{s}$	I_{LM}	±3.9	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	-0.4	A
ESD Rating, MIL-STD-883D HBM (100 pF, 1.5 k Ω)		ESD	3.0	kV
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	320	$^\circ\text{C}/\text{W}$
Junction-to-Foot – Steady State (Note 1)	$R_{\theta JF}$	220	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

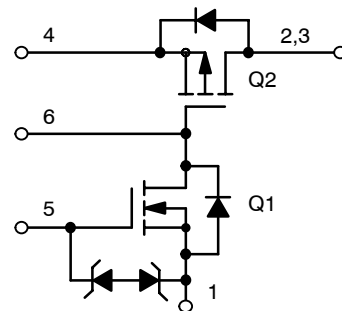


ON Semiconductor®

<http://onsemi.com>

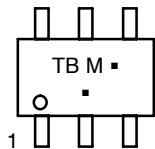
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
8.0 V	130 m Ω @ -4.5 V	±1.3 A
	170 m Ω @ -2.5 V	
	260 m Ω @ -1.8 V	

SIMPLIFIED SCHEMATIC



SC-88
(SOT-363)
CASE 419B
STYLE 30

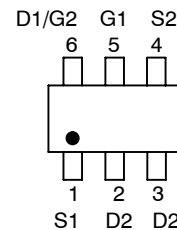
MARKING DIAGRAM



TB = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTJD1155LT1	SC-88	3000/Tape & Reel
NTJD1155LT1G	SC-88 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTJD1155L

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	
OFF CHARACTERISTICS							
Q2 Drain-to-Source Breakdown Voltage	V_{IN}	$V_{GS2} = 0\text{ V}, I_{D2} = 250\ \mu\text{A}$	-8.0			V	
Forward Leakage Current	I_{FL}	$V_{GS1} = 0\text{ V}, V_{DS2} = -8.0\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA	
			$T_J = 125^\circ\text{C}$		10		
Q1 Gate-to-Source Leakage Current	I_{GSS}	$V_{DS1} = 0\text{ V}, V_{GS1} = \pm 8.0\text{ V}$			± 100	nA	
Q1 Diode Forward On-Voltage	V_{SD}	$I_S = -0.4\text{ A}, V_{GS1} = 0\text{ V}$		-0.8	-1.1	V	
ON CHARACTERISTICS							
ON/OFF Voltage	$V_{ON/OFF}$		1.5		8.0	V	
Q1 Gate Threshold Voltage	$V_{GS1(th)}$	$V_{GS1} = V_{DS1}, I_D = 250\ \mu\text{A}$	0.4		1.0	V	
Input Voltage	V_{IN}	$V_{GS1} = V_{DS1}, I_D = 250\ \mu\text{A}$	1.8		8.0	V	
Q2 Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{ON/OFF} = 1.5\text{ V}$	$V_{IN} = 4.5\text{ V}$ $I_L = 1.2\text{ A}$		130	175	m Ω
			$V_{IN} = 2.5\text{ V}$ $I_L = 1.0\text{ A}$		170	220	
			$V_{IN} = 1.8\text{ V}$ $I_L = 0.7\text{ A}$		260	320	
Load Current	I_L	$V_{DROP} \leq 0.2\text{ V}, V_{IN} = 5.0\text{ V}, V_{ON/OFF} = 1.5\text{ V}$	1.0			A	
		$V_{DROP} \leq 0.3\text{ V}, V_{IN} = 2.5\text{ V}, V_{ON/OFF} = 1.5\text{ V}$	1.0				

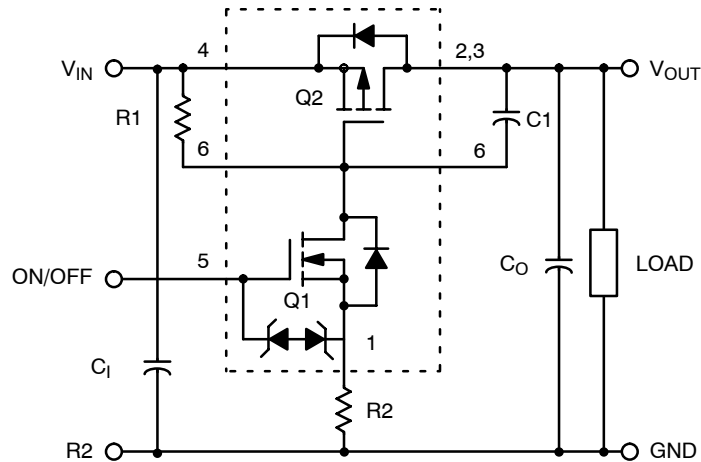


Figure 1. Load Switch Application

Components	Description	Values
R1	Pullup Resistor	Typical 10 k Ω to 1.0 M Ω *
R2	Optional Slew-Rate Control	Typical 0 to 100 k Ω *
C_0, C_1	Output Capacitance	Usually < 1.0 μF
C1	Optional In-Rush Current Control	Typical $\leq 1000\ \text{pF}$

*Minimum R1 value should be at least 10 x R2 to ensure Q1 turn-on.

NTJD1155L

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

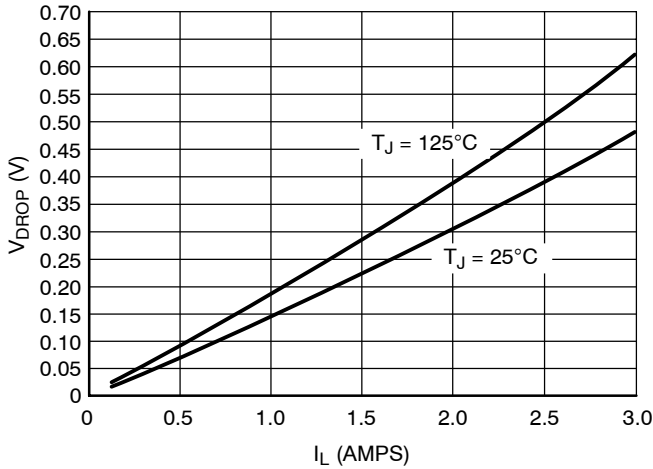


Figure 2. V_{drop} vs. I_L @ $V_{\text{in}} = 2.5 \text{ V}$

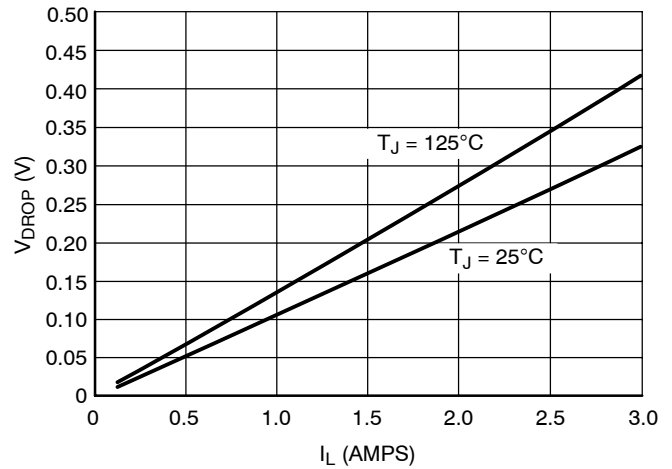


Figure 3. V_{drop} vs. I_L @ $V_{\text{in}} = 4.5 \text{ V}$

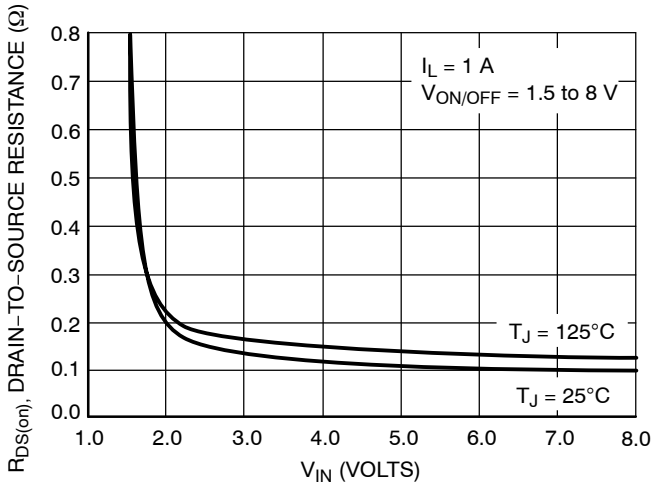


Figure 4. On-Resistance vs. Input Voltage

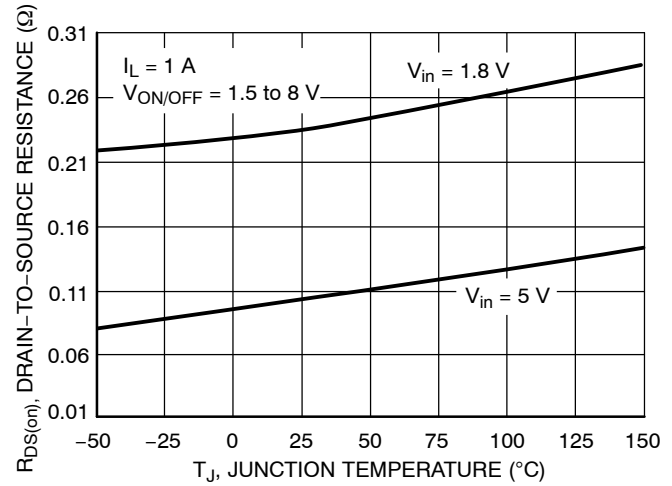


Figure 5. On-Resistance Variation with Temperature

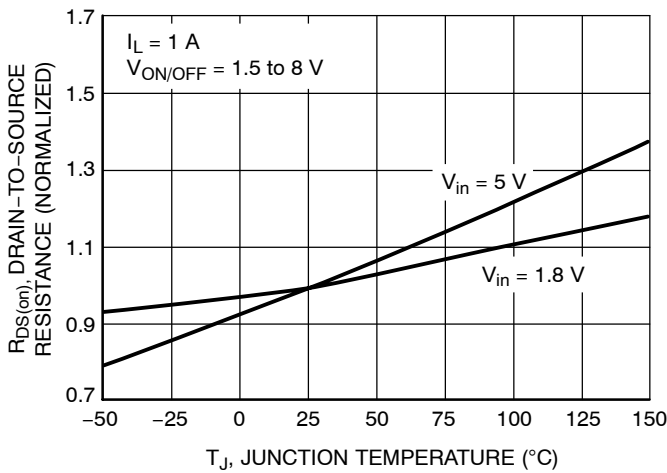


Figure 6. Normalized On-Resistance Variation with Temperature

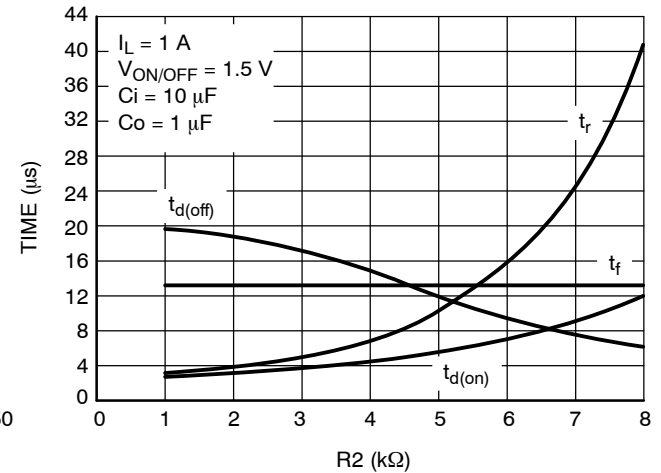


Figure 7. Switching Variation $R2$ @ $V_{\text{in}} = 4.5 \text{ V}$, $R1 = 20 \text{ k}\Omega$

NTJD1155L

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

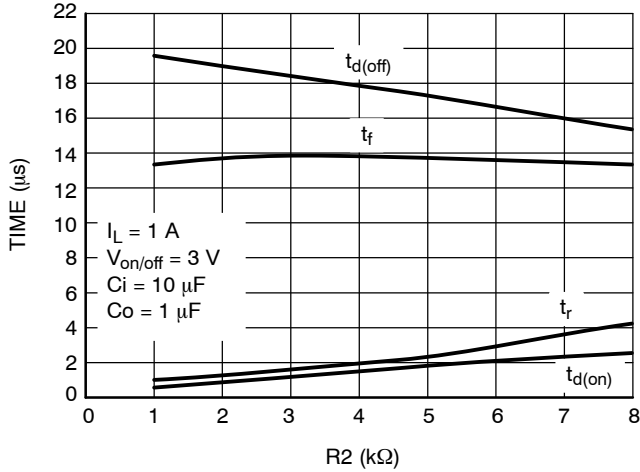


Figure 8. Switching Variation
R2 @ $V_{in} = 4.5\text{ V}$, $R1 = 20\ \text{k}\Omega$

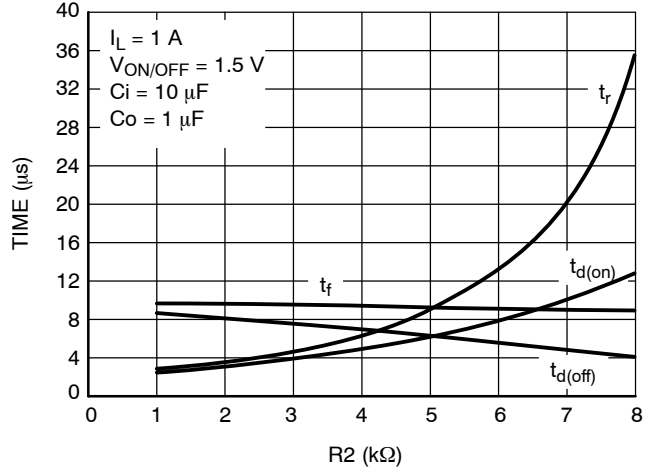


Figure 9. Switching Variation
R2 @ $V_{in} = 2.5\text{ V}$, $R1 = 20\ \text{k}\Omega$

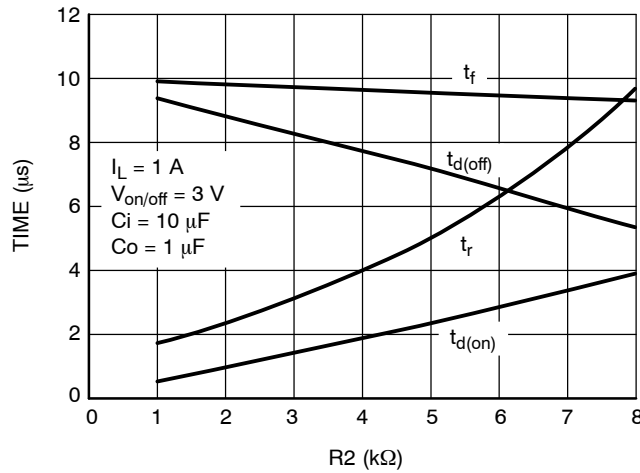


Figure 10. Switching Variation
R2 @ $V_{in} = 2.5\text{ V}$, $R1 = 20\ \text{k}\Omega$

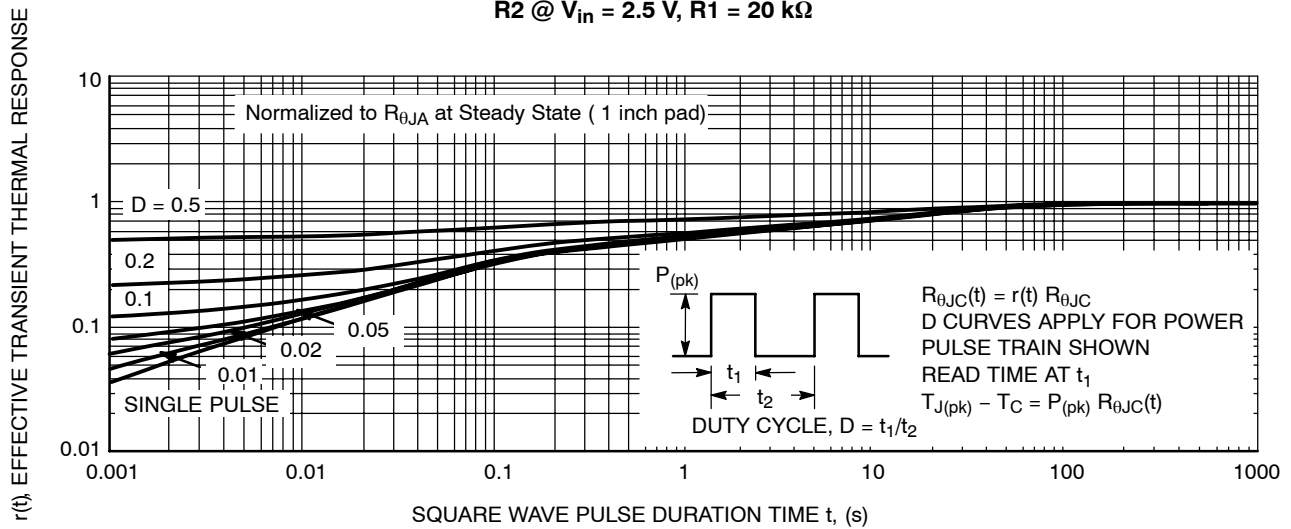
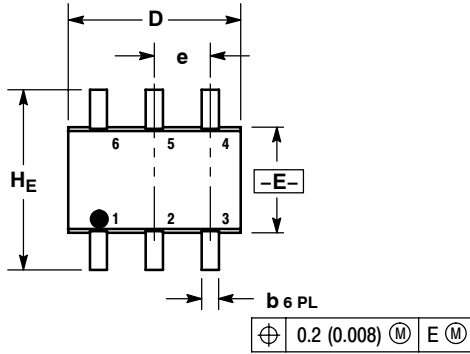


Figure 11. FET Thermal Response

NTJD1155L

PACKAGE DIMENSIONS

SC-88 (SOT-363)
CASE 419B-02
ISSUE W



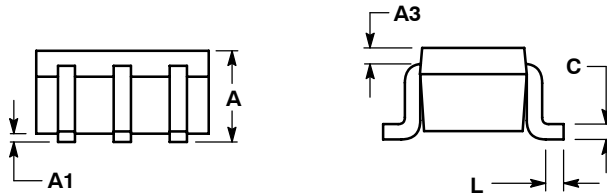
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

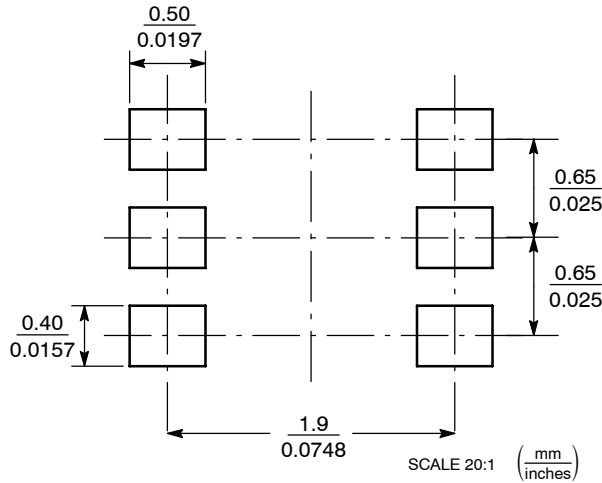
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	2.00	2.10	2.20	0.078	0.082	0.086

STYLE 30:

- PIN 1. SOURCE 1
- DRAIN 2
- DRAIN 2
- SOURCE 2
- GATE 1
- DRAIN 1



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>
Order Literature: <http://www.onsemi.com/litorder>
For additional information, please contact your local Sales Representative.